Verilog:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 07/20/2022 09:56:02 AM

// Design Name:

// Module Name: tflipflop

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module tflipflop(

input t,

input clk,

input rst,

output z

);

reg CS, NS;

parameter zero = 0;

parameter one = 1;

always @ (posedge clk, negedge rst) begin

if (rst == 1'b0) begin NS <= 0; end

else begin

CS <= NS; end

end

always@(CS, t) begin

case(CS)

zero: NS = t? one : zero;

one: NS = t? zero : one;

default: NS = zero;

endcase

end

assign z = (CS == one);

endmodule

Test bench

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 07/20/2022 10:18:39 AM

// Design Name:

// Module Name: tflipflop\_tb

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module tflipflop\_tb;

reg t, clk;

wire z;

tflipflop UUT(

.z(z),

.t(t),

.clk(clk));

initial begin

clk = 0;

forever #5 clk = ~clk;

end

initial begin

$monitor("z = ", z);

#2 t = 0; #10 t = 1; #20 t = 0; #10 t = 1;

#10 $finish;

end

endmodule